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APPLICATION

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TITLE: MULTILAYERED PHASE CHANGE MEMORY

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MULTILAYERED PHASE CHANGE MEMORY

Background

This invention relates generally to phase change memories.

Phase change memory devices use phase change
5 materials, i.e., materials that may be electrically
switched between a generally amorphous and a generally
crystalline state, as an electronic memory. One type of
memory element utilizes a phase change material that may
be, in one application, electrically switched between
10 generally amorphous and generally crystalline local orders
or between the different detectable states of local order
across the entire spectrum between completely amorphous and
completely crystalline states.

Typical materials suitable for such an application
15 include various chalcogenide elements. The state of the
phase change materials is also non-volatile. When the
memory is set in either a crystalline, semi-crystalline,
amorphous, or semi-amorphous state representing a
resistance value, that value is retained until
20 reprogrammed, even if power is removed. This is because
the program value represents a phase or physical state of
the memory (e.g., crystalline or amorphous).

Thus, there is a need for alternate ways to form phase
change memories.

Brief Description of the Drawings

Figure 1 is a partially cross-sectional and partially schematic depiction of one embodiment of the present invention;

5 Figure 2 is a partially cross-sectional and a partially schematic view of another embodiment of the present invention;

 Figure 3 is a partially cross-sectional and partially schematic view of still another embodiment of the present
10 invention; and

 Figure 4 is a system depiction of one embodiment of the present invention.

Detailed Description

Referring to Figure 1, a phase change memory may
15 include a cell 10. The cell 10 may be accessed by a pair of conductive lines including the line 12, which is coupled selectively to the cell 10 by a selection device 14. The selection device 14 may also be called an access device or an isolation device. The selection device 14, in one
20 embodiment, may be formed in a semiconductor substrate 28. As examples, the selection device 14 may be a transistor or a diode. The lines 12 may be address lines that may be used to address one cell in an array of cells, addressable using said lines 12, for reading or programming.

25 A pore or opening may be defined in an insulating layer 18 formed over the substrate 28. The pore may

include a lower electrode 16 coupled to the selection device 14 and upper electrode 20 coupled to another conductive line (not shown). In one embodiment, one conductive line 12 extends in a first direction and the
5 other conductive line extends transversely thereto. The conductive lines may also be known as rows and columns.

Between the upper electrode 20 and the lower electrode 16 is an active phase change memory layer 24 which acts as the memory medium for the cell 10. Above the layer 24 is a
10 chalcogenide or ovonic layer 26. A chalcogenide or ovonic layer 22 is positioned below the layer 24.

The layers 22 and 26 may be crystalline chalcogenide alloys designed to resist transformation into the glassy structural state in one embodiment. Thus, the layers 22
15 and 26 may be termed non-switching layers because in operation they do not change resistance due to change of phase or high field switching. Thus, the non-switching layers 22 and 26 may be called a stable structural phase. Alloys of permanently lower resistivity chalcogenide
20 material may be used as the layers 22, 26. The layers 22, 26 may interface directly to the active phase change memory layer 24, providing resistive heating, as well as high thermal isolation of the active programmable volume within the layer 24. In one embodiment, the layers 22 and 26 may
25 have a resistivity in the range of 10 to 100 Mohm centimeter.

Because of the resistivity supplied by the layers 22 and 26, more uniform current and better thermal isolation may be delivered to the sandwiched active phase change material layer 24 in one embodiment. This may reduce micro
5 filamentation during programming of the phase change memory cell 10.

The active phase change layer 24 may be sandwiched between symmetrical top and bottom electrode systems, each including a non-switching layer 22 or 26 and an electrode
10 16 or 20. Heat loss prevention during phase change may be enhanced by the high thermal insulating properties of the layers 22 and 26 in some embodiments. The chemical similarity of the layers 22 and 26 to layer 24 provides for strong adhesion, integrity, and encapsulation in some
15 embodiments. *In situ* deposition of all three layers 22, 24, and 26 may further improve the interfaces of electrode to phase change elements in some embodiments.

A crystalline chalcogenide alloy designed to resist phase transformation may be used for the layers 22 and 26
20 and to provide electrical contacts to the active phase change material layer 24. Examples of materials that may be utilized for the layer 22 and 26 include materials of the form As_xSe_y where X is 2 or 9 and Y is 3.

In one embodiment, the phase change material for the
25 layer 24 may be a non-volatile, phase change material. A phase change material may be a material having electrical properties (e.g., resistance) that may be changed through

the application of energy such as, for example, heat, light, voltage potential, or electrical current.

Examples of phase change materials may include a chalcogenide material or an ovonic material. An ovonic material may be a material that undergoes electronic or structural changes and acts as a semiconductor once subjected to application of a voltage potential, electrical current, light, heat, etc. A chalcogenide material may be a material that includes at least one element from column VI of the periodic table or may be a material that includes one or more of the chalcogen elements, e.g., any of the elements of tellurium, sulfur, or selenium. Ovonic and chalcogenide materials may be non-volatile memory materials that may be used to store information. Ovonic or chalcogenide materials may be used to form the layers 22 and 26.

In one embodiment, the memory material for the layer 24 may be chalcogenide element composition from the class of tellurium-germanium-antimony ($\text{Te}_x\text{Ge}_y\text{Sb}_z$) material or a GeSbTe alloy, although the scope of the present invention is not limited to just these materials.

In one embodiment, if the memory material for the layer 24 is a non-volatile, phase change material, the memory material may be programmed into one of at least two memory states by applying an electrical signal to the memory material. An electrical signal may alter the phase of the memory material between a substantially crystalline

state and a substantially amorphous state, wherein the electrical resistance of the memory material in the substantially amorphous state is greater than the resistance of the memory material in the substantially crystalline state. Accordingly, in this embodiment, the memory material may be adapted to be altered to one of at least two resistance values within a range of resistance values to provide single bit or multi-bit storage of information.

10 Programming of the memory material in the layer 24 to alter the state or phase of the material may be accomplished by applying voltage potentials to the line 12 and electrode 20, thereby generating a voltage potential across the memory material layer 24. An electrical current
15 may flow through a portion of the memory material layer 24 in response to the applied voltage potentials, and may result in heating of the memory material layer 24.

 This heating and subsequent cooling may alter the memory state or phase of the memory material layer 24.
20 Altering the phase or state of the memory material layer 24 may alter an electrical characteristic of the memory material layer 24. For example, resistance of the material layer 24 may be altered by altering the phase of the memory material layer 24. The memory material may also be
25 referred to as a programmable resistive material or simply a programmable material.

In one embodiment, a voltage potential difference of about 3 volts may be applied across a portion of the memory material by applying about 3 volts to a lower line 12 and about zero volts to an upper electrode 20. A current
5 flowing through the memory material layer 24 in response to the applied voltage potentials may result in heating of the memory material. This heating and subsequent cooling may alter the memory state or phase of the material.

In a "reset" state, the memory material in the layer
10 24 may be in an amorphous or semi-amorphous state and in a "set" state, the memory material may be in a crystalline or semi-crystalline state. The resistance of the memory material in the amorphous or semi-amorphous state may be greater than the resistance of the material in the
15 crystalline or semi-crystalline state. The association of reset and set with amorphous and crystalline states, respectively, is a convention. Other conventions may be adopted.

Due to electrical current, the memory material in the
20 layer 24 may be heated to a relatively higher temperature to amorphize memory material and "reset" memory material (e.g., program memory material to a logic "0" value). Heating the volume or memory material to a relatively lower crystallization temperature may crystallize memory material
25 and "set" memory material (e.g., program memory material to a logic "1" value). Various resistances of memory material may be achieved to store information by varying the amount

of current flow and duration through the volume of memory material.

The information stored in memory material layer 24 may be read by measuring the resistance of the memory material. As an example, a read current may be provided to the memory material using opposed line 12 and electrode 20 and a resulting read voltage across the memory material may be compared against a reference voltage using, for example, a sense amplifier (not shown). The read voltage may be proportional to the resistance exhibited by the memory storage element. Thus, a higher voltage may indicate that memory material is in a relatively higher resistance state, e.g., a "reset" state. A lower voltage may indicate that the memory material is in a relatively lower resistance state, e.g., a "set" state.

Referring to Figure 2, in accordance with another embodiment of the present invention, a non-switching cup-shaped material 26a may be filled with an insulator 18, such as oxide. The active phase change memory layer 24 may be sandwiched between layers 22 and 26, which may be a non-switching phase change material and the layer 28. The layer 28 may be an electrically insulating nitride encapsulation layer in one embodiment of the present invention. For the non-switching cup-shaped material layer 26a to connect to layer 18, an etch through the layer 18 may be used. The material 26a may be a chalcogenide or

ovonic material of the form As_xSe_y , where X is 2 or 9 and Y is 3, for example.

In accordance with still another embodiment of the present invention, shown in Figure 3, a non-switching material layer 22a may be non-planar and in one embodiment, the non-switching layer 22a may be U-shaped. The active or switching phase change memory layer 24 may be contained within the U-shaped layer 22a in one embodiment. The non-switching layer 26b may be formed over an insulating layer 18 which has been shaped into a sub-lithographic opening size by a spacer process, for example. The non-switching layer 26b is made to contact the active switching layer 24 and serve as an electrode. A conductor 20a may be deposited over the layer 26b to provide an upper electrical connection. The layers 22a and 26b may be a chalcogenide or ovonic material of the form As_xSe_y , where X is 2 or 9 and Y is 3, for example.

In some embodiments, the layers 22 and 26 may be permanently of a low resistivity to make a good ohmic contact to the active switching layer 24. In some other embodiments a higher resistivity layer 22 or 26 is selected to achieve resistive heating to assist in heating the active switching material layer 24 to produce phase change. The layers 22 and 26 may not switch between conductive and resistive states. The layers 22 and 26 may provide, in some cases, resistive heating, higher thermal insulation, more uniform current, stronger adhesion to the switching

layer 24, and the ability to use the same deposition chamber for all three layers. This may increase cleanliness and improve throughput.

Turning to Figure 4, a portion of a system 500 in accordance with an embodiment of the present invention is described. System 500 may be used in wireless devices such as, for example, a personal digital assistant (PDA), a laptop or portable computer with wireless capability, a web tablet, a wireless telephone, a pager, an instant messaging device, a digital music player, a digital camera, or other devices that may be adapted to transmit and/or receive information wirelessly. System 500 may be used in any of the following systems: a wireless local area network (WLAN) system, a wireless personal area network (WPAN) system, or a cellular network, although the scope of the present invention is not limited in this respect.

System 500 may include a controller 510, an input/output (I/O) device 520 (e.g. a keypad, display), a memory 530, and a wireless interface 540 coupled to each other via a bus 550. It should be noted that the scope of the present invention is not limited to embodiments having any or all of these components.

Controller 510 may comprise, for example, one or more microprocessors, digital signal processors, microcontrollers, or the like. Memory 530 may be used to store messages transmitted to or by system 500. Memory 530 may also optionally be used to store instructions that are

executed by controller 510 during the operation of system 500, and may be used to store user data. Memory 530 may be provided by one or more different types of memory. For example, memory 530 may comprise a volatile memory (any
5 type of random access memory), a non-volatile memory such as a flash memory, and/or phase change memory that includes a cell such as, for example, the cell 10 illustrated in Figure 1 which may employ non-switching chalcogenide electrode layers 22, 26 in one embodiment.

10 The I/O device 520 may be used to generate a message. The system 500 may use the wireless interface 540 to transmit and receive messages to and from a wireless communication network with a radio frequency (RF) signal. Examples of the wireless interface 540 may include a
15 wireless transceiver or an antenna, such as a dipole antenna, although the scope of the present invention is not limited in this respect.

While the present invention has been described with respect to a limited number of embodiments, those skilled
20 in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

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